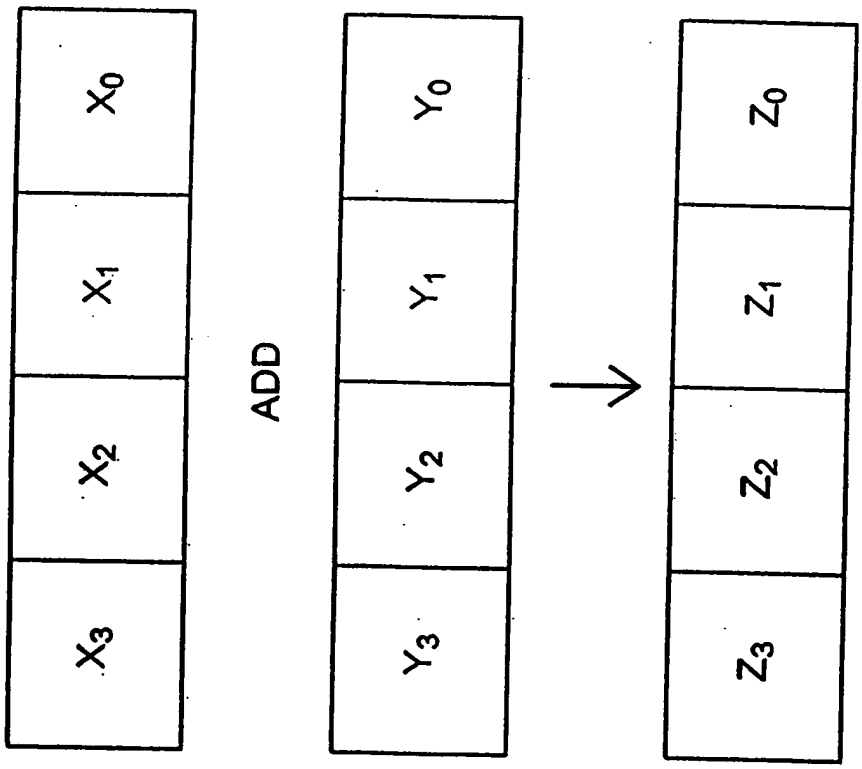

FIG. 1
PRIOR ART

TIME	ADD X, Y	ADD A, B	MUL X, Y	ADD S, T
T	T + 1	T + 2	T + 3	

FIG. 2B

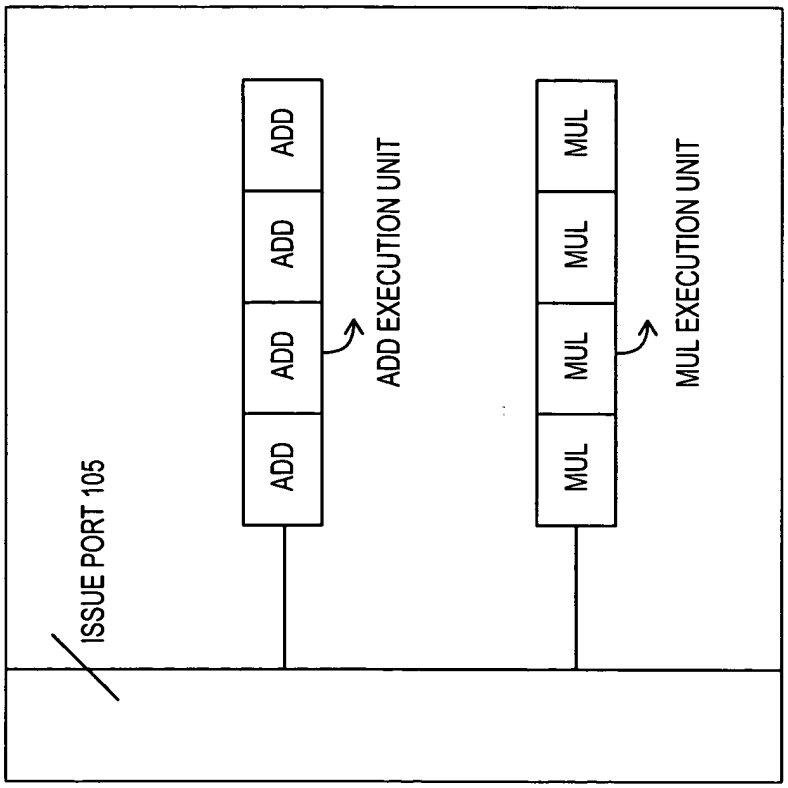

FIG. 2A

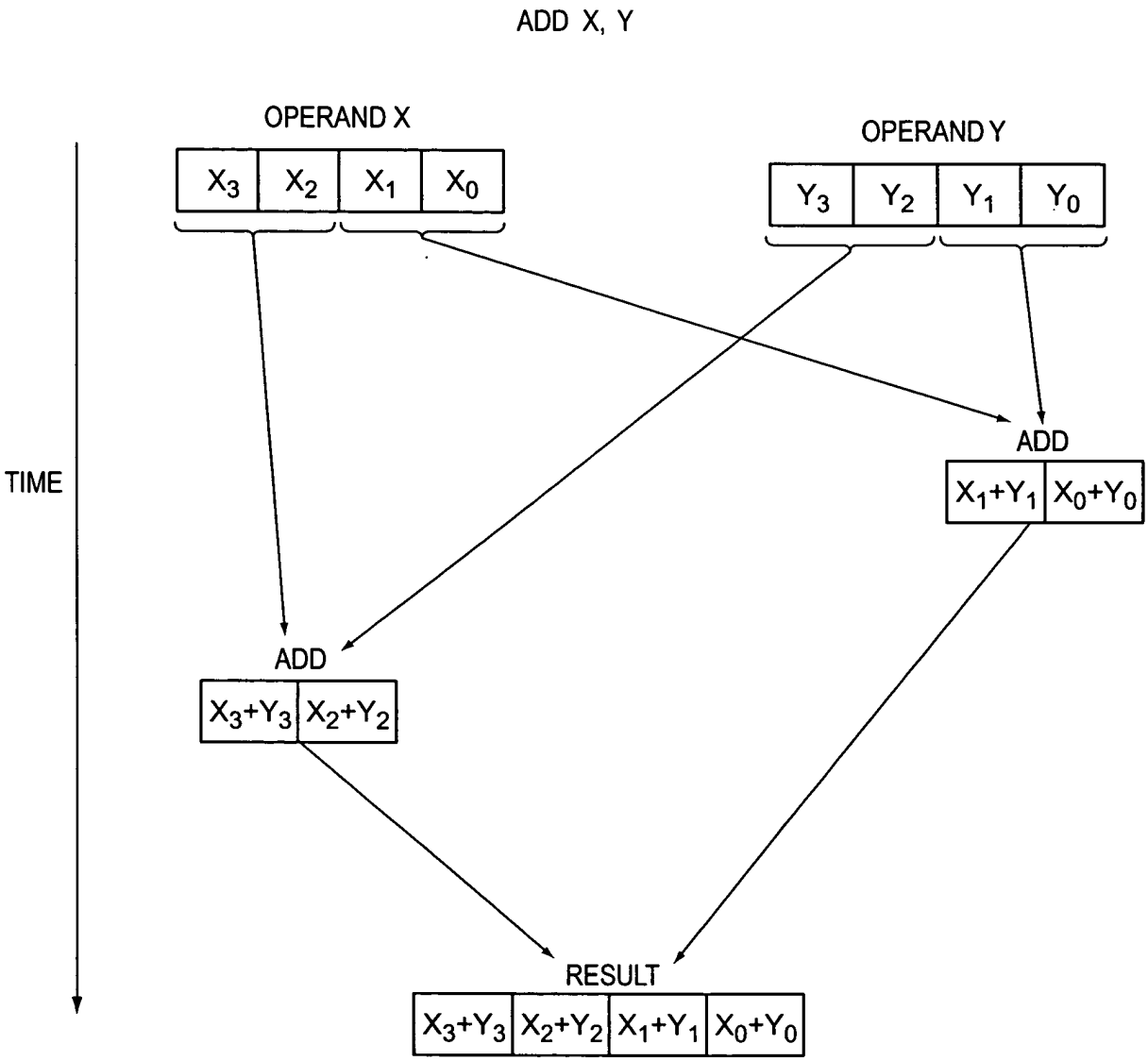
ADD X, Y
OPERAND X
X3 X2 X1 X0
OPERAND Y
Y3 Y2 Y1 Y0
TIME
ADD
X1+Y1 X0+Y0
ADD
X3+Y3 X2+Y2
RESULT
X3+Y3 X2+Y2 X1+Y1 X0+Y0

FIG. 3

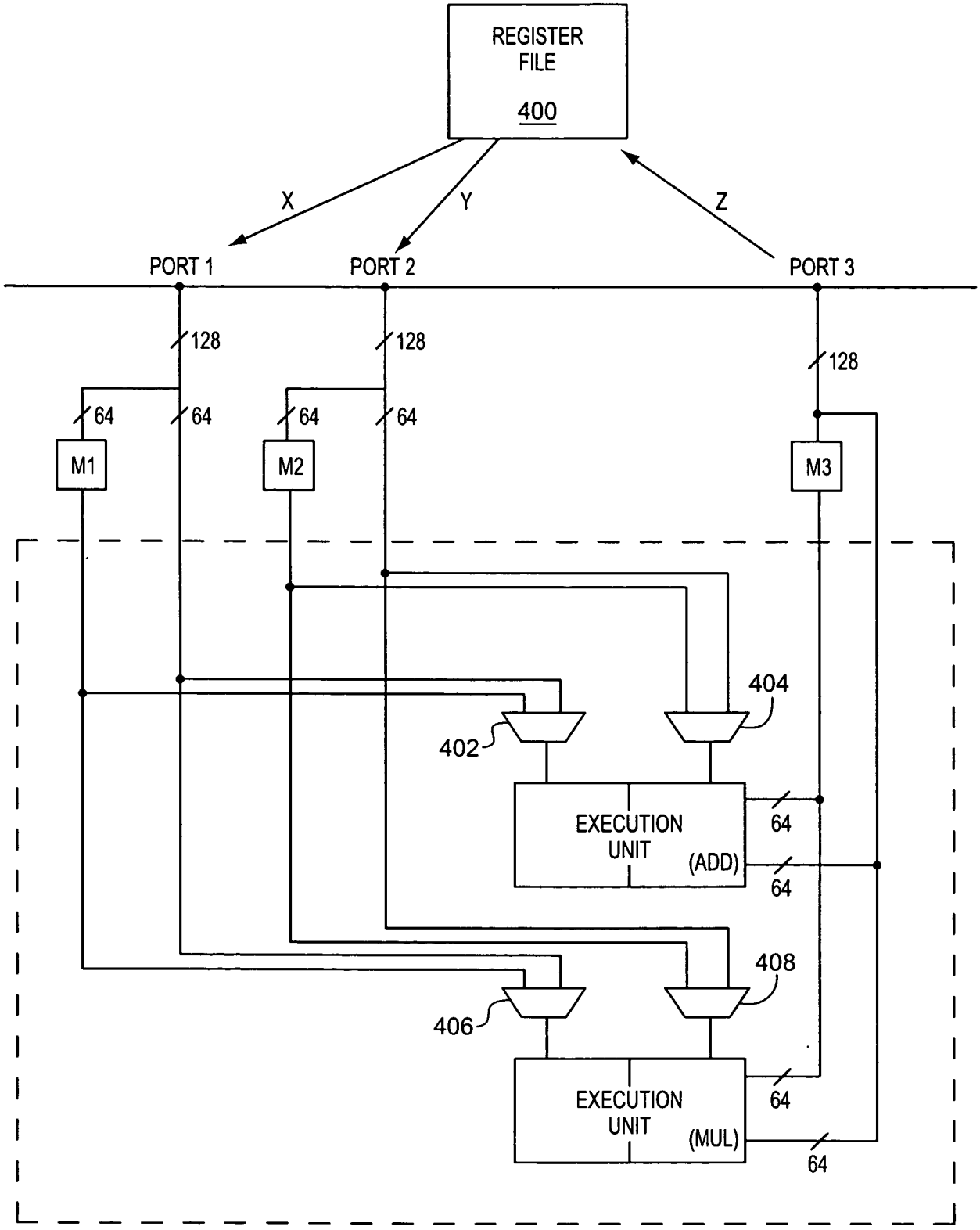
REGISTER FILE
400
X
Y
Z
PORT 1
PORT 2
PORT 3
128
128
128
64
64
64
64
M1
M2
M3
404
402
EXECUTION UNIT
(ADD)
64
64
408
406
EXECUTION UNIT
(MUL)
64
64

FIG. 4A

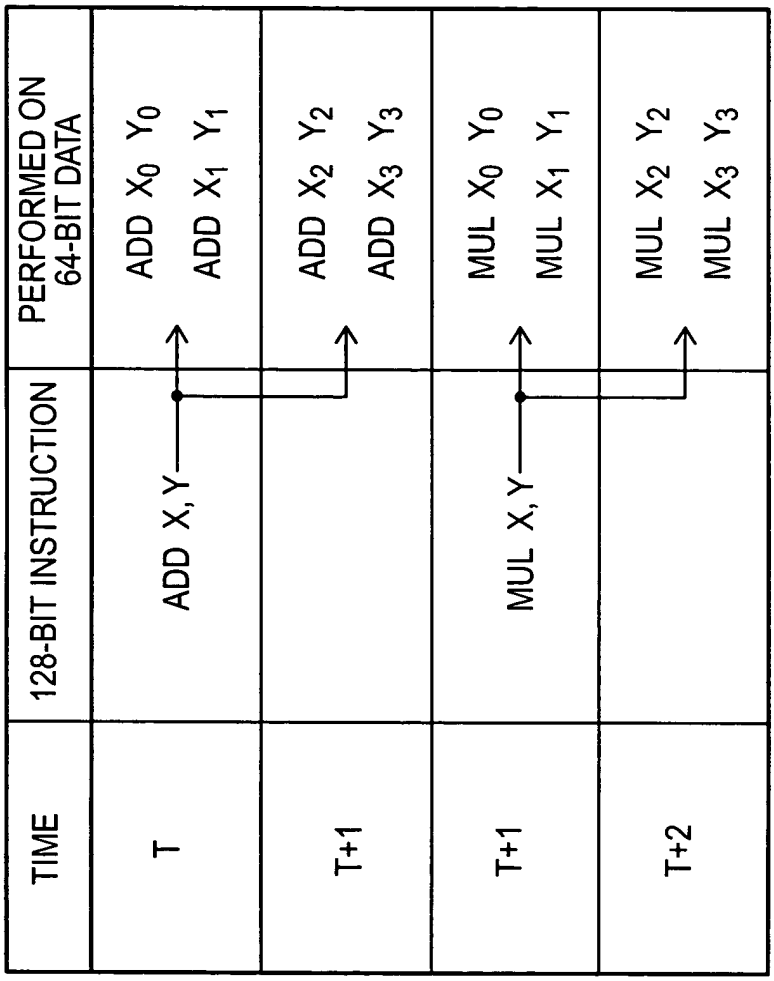
TIME
128-BIT INSTRUCTION
PERFORMED ON 64-BIT DATA
T
ADD X, Y
ADD X0 Y0
ADD X1 Y1
T+1
ADD X2 Y2
ADD X3 Y3
T+1
MUL X, Y
MUL X0 Y0
MUL X1 Y1
T+2
MUL X2 Y2
MUL X3 Y3

FIG. 4B

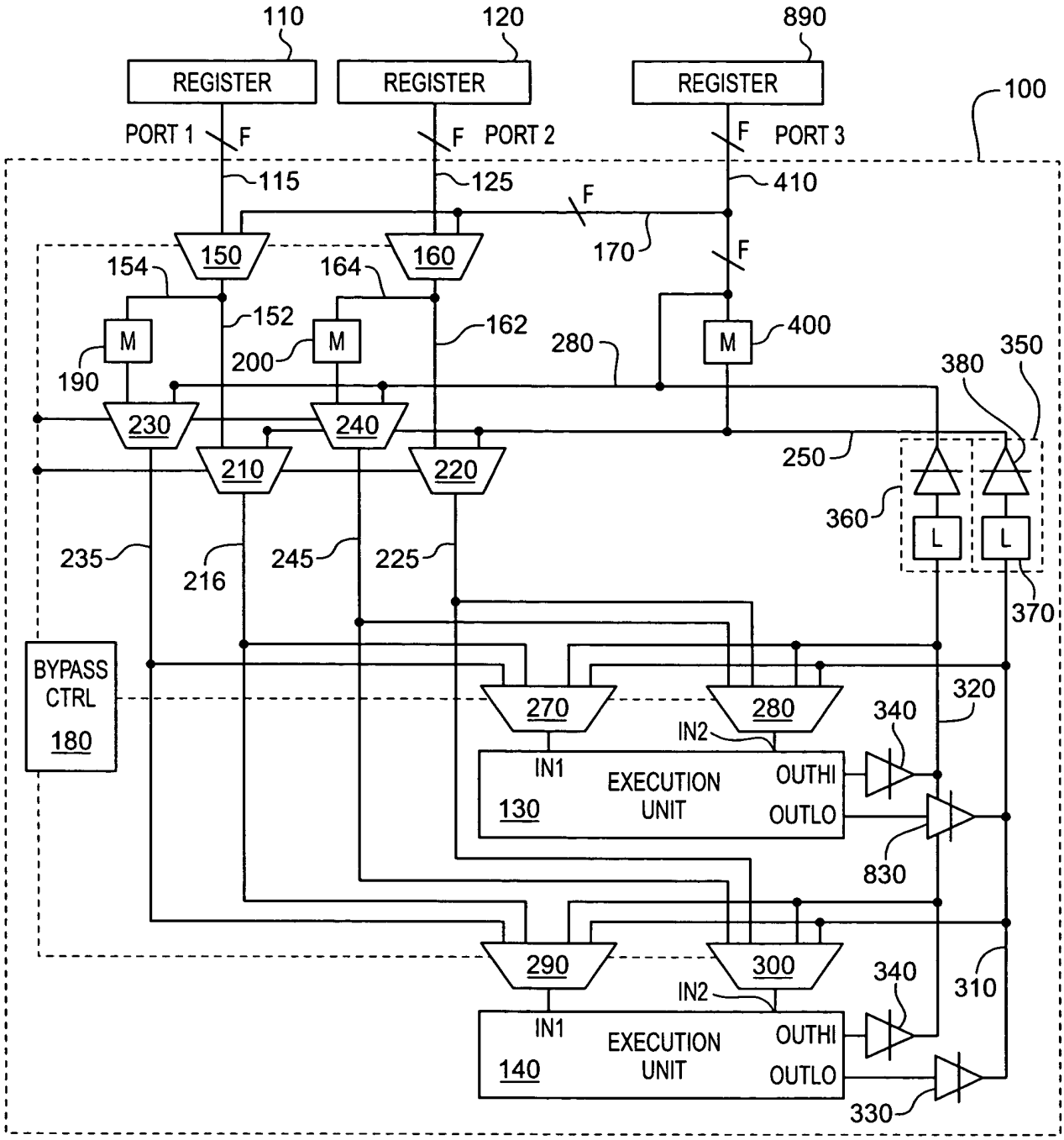
110
120
890
REGISTER
REGISTER
REGISTER
100
PORT 1
F
F
PORT 2
F
PORT 3
115
125
410
F
170
F
150
160
154
164
152
162
280
M
M
M
400
190
200
380
350
230
240
250
210
220
360
L
L
235
216
245
225
370
BYPASS CTRL
180
270
280
320
340
IN2
IN1
EXECUTION UNIT
130
OUTHI
OUTLO
830
290
300
340
310
IN2
IN1
EXECUTION UNIT
140
OUTHI
OUTLO
330

FIG. 5

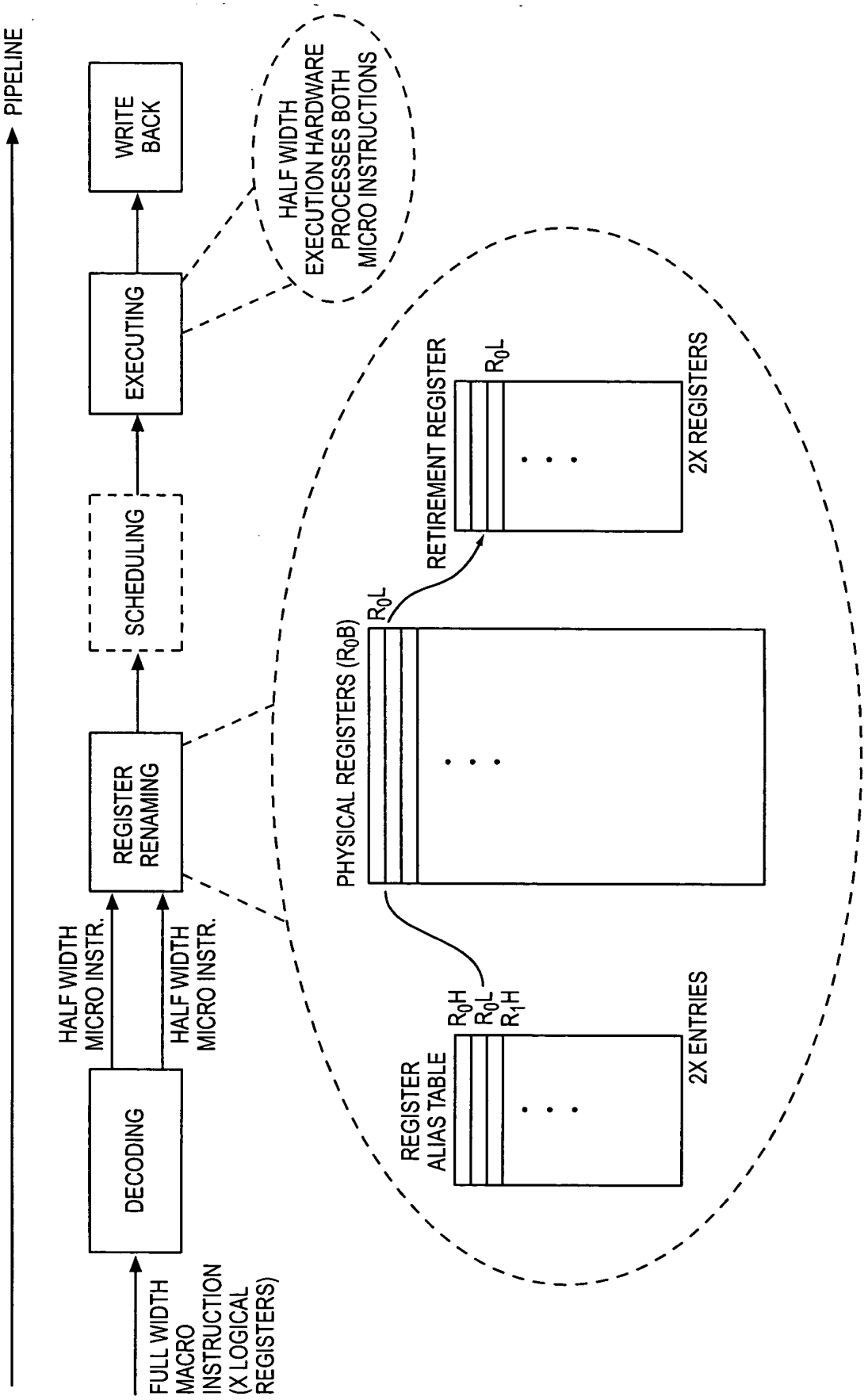
PIPELINE
FULL WIDTH MACRO INSTRUCTION (X LOGICAL REGISTERS)
DECODING
HALF WIDTH MICRO INSTR.
HALF WIDTH MICRO INSTR.
REGISTER RENAMING
SCHEDULING
EXECUTING
WRITE BACK
HALF WIDTH EXECUTION HARDWARE PROCESSES BOTH MICRO INSTRUCTIONS
REGISTER ALIAS TABLE
R_0H R_0L R_1H
2X ENTRIES
PHYSICAL REGISTERS (R_0B)
R_0L
RETIREMENT REGISTER
R_0L
2X REGISTERS

FIG. 6A

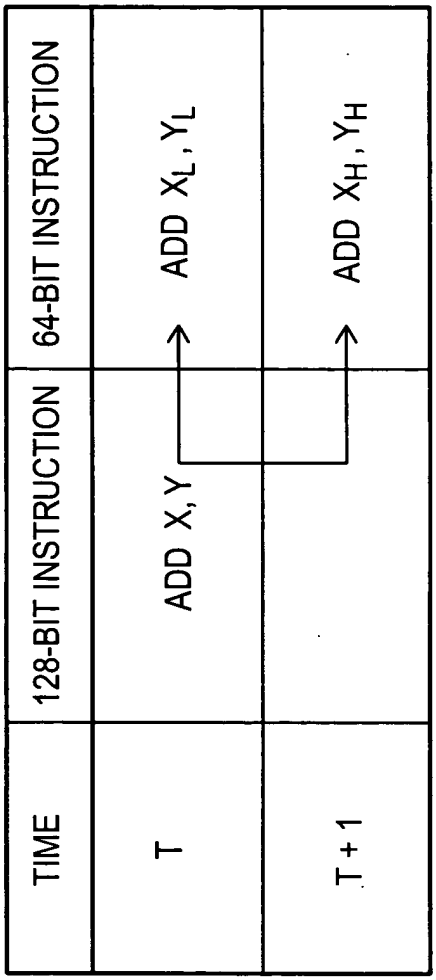
TIME
128-BIT INSTRUCTION
64-BIT INSTRUCTION
T
ADD X, Y
ADD X_L, Y_L
ADD X_H, Y_H
T + 1

FIG. 6B